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EXAMINER
MOE, AUNG SOE

ART UNIT	PAPER NUMBER
2612	14

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/327,523	Applicant(s) Ueno et al.
	Examiner Aung Moe	Art Unit 2612

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Apr 30, 2003*

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above, claim(s) *9-11* is/are withdrawn from consideratio

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-8 and 12-15* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Jun 8, 1999* is/are a) ☐ accepted or b) ☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examine

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *8*
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restriction

1. Applicant's election with traverse of Species I (Figs. 1-9) and claims 1-8 and 12-15 in Paper No. 13 (received on 4/30/03) is acknowledged. The traversal is on the ground(s) that "no serious burden would be placed upon the Examiner if all claims were simultaneously examined as search and examination of one of the species would inherently duplicate the search required for examination of the other species". This is not found persuasive because it is noted that the most recent restriction requirement made was in the form of an election of Species, not a restriction requirement between more than one invention.

Moreover, the invention which is elected by the Applicant (i.e., Group I of Figs 1-9) is disclosed in the specification and drawings for being embodied in multiple **patentably distinct** embodiments (i.e., noted that Figs. 10-16C are directed to different type of sensor arrangements than the elected Species of figures 1-9). In view of this, the mere evidence of several patentably distinct embodiments is ***prima facie*** evidence of examining burdens of the Examiner.

The requirement is still deemed proper and is therefore made FINAL.

Drawings

2. Figure 18 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. Figure 7 is objected to as failing to comply with 37 CFR 1.84(p)(4) because, as shown in Fig. 7, the reference character "ϕTn" corresponding to the signal line 26 should be labeled as "ϕRn" (i.e., noted that switch 14 is for Reset) and the reference character "ϕRn" corresponding to the signal line 25 should be label as "ϕTn" (i.e., noted that switch 12 is for Transfer; see Figs. 7-8 and page 19, lines 2+ of the specification).

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 1-8 are objected to because of the following informalities:

In claim 1, please change the word "pixels" as recited in line 11 to -- said pixels -- because the word "pixels" have been mentioned in line 2 of claim 1.

In claim 2, please change the words "a reset" as recited in line 4 to -- said reset --, because the phrase "a reset potential" has been mentioned in line 12 of claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3, 5-7, 12-14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Gowda et al. (U.S. 5,898,168).

Regarding claim 1, Gowda '168 discloses a solid-state imaging element (Figs. 2 and 3A), comprising: unit pixels (18/30), arranged in a matrix form, which have photoelectric transfer elements (26), transfer switches (Figs. 1 and 3B; the elements' 8 and 22; see col. 1, lines 30+ and col. 4, lines 20+) for transferring charges stored in said photoelectric transfer elements (26), charge store parts (i.e., Figs. 1 and 3B; the elements' 7 and 25; col. 1, lines 65+ and col. 5, lines 50+) for storing charges transferred by said transfer switches (i.e., 8/22), reset switches (Figs. 1

and 3B; the elements' 11 and 21) for resetting said charge store parts (i.e., 7/25), and amplifying elements (i.e., Fig. 1 and 3B; the elements' 13 and 23; see col. 2, lines 10+) for outputting signals in accordance with the potential of said charge store part to vertical signal lines (i.e., Figs. 1 and 3B; the element 15 and 15j);

a vertical scanning circuit (Figs. 2 and 3, the elements' 14 and 14') for selecting the pixels in units (18/30) of rows by controlling a reset potential afforded to said reset switches (11/21; see Figs. 5-6 and 11 and col. 4, lines 30+);

a horizontal scanning circuit (Figs. 2 and 3A; the elements' 28 and 31_1 to 31_N; col. 1, lines 50+ col. 4, lines 15+, and col. 5, lines 30+) for sequentially selecting signals output to said vertical signal lines (15/15j) in units of columns (i.e., see col. 4, lines 35+); and

an output circuit (i.e., Figs. 2 and 3A; the elements' 31_1 to 31_N and 16; col. 1, lines 50+ and col. 6, lines 8+) for outputting signals selected by said horizontal scanning circuit via horizontal signal lines (i.e., noted the bus lines connected between the elements 28 and 31 as shown in Figs. 2 and 3A).

Regarding claim 2, Gowda '168 discloses wherein said vertical scanning circuit affords vertical selection pulses sequentially output during vertical scanning to said reset switches as a reset potential thereof (i.e., see col. 4, lines 30+ and col. 5, lines 15+).

Regarding claim 3, Gowda '168 discloses wherein said charge stored part is floating diffusion (i.e., col. 1, lines 65+).

Regarding claim 5, Gowda '168 discloses wherein said output circuit outputs signals read into said vertical signal lines (15/15j) in voltage mode (i.e., "VOUT"; see col. 8, lines 20-25).

Regarding claim 6, Gowda '168 discloses wherein said output circuit outputs signals read into said vertical signal lines in current mode (i.e., col. 7, lines 39+).

Regarding claim 7, Gowda '168 discloses wherein said unit pixels (18/30) include an overflow (i.e., Fig. 14; the element 92) path between said photoelectric transfer element (110) and an area to which a pixel source voltage is afforded (i.e., VDD), said overflow path being used to discharge excess charges of said photoelectric transfer element (i.e., col. 10, lines 15-32).

Regarding claim 12, Gowda '168 discloses a method for driving a solid-state imaging element (Figs. 2 and 3A) including unit pixels, arranged in a matrix form (18/30), which have photoelectric transfer elements (6/26), transfer switches (8/22) for transferring charges stored in said photoelectric transfer elements (6/26), charge stored parts for storing charges (i.e., Figs. 1 and 3B; the elements' 7 and 25; col. 1, lines 65+ and col. 5, lines 50+) transferred by said transfer switches (8/22), reset switches (11/21) for resetting said charge store parts (i.e., 7/25), and amplifying elements (i.e., 13/23) for outputting signals in accordance with the potential of said charge store parts to vertical signals lines (i.e., 15/15j), said method comprising the step of:

selecting pixels in units of rows by controlling a reset potential afforded to said reset switches (i.e., see Figs. 5-6 and 11; col. 4, lines 25+ and col. 5, lines 20+).

Regarding claim 13, Gowda '168 discloses the step of: outputting signals read into said vertical signal lines in voltage mode (i.e., col. 8, lines 21+).

Regarding claim 14, Gowda '168 discloses the step of: outputting signals read into said vertical signal lines in current mode (i.e., col. 7, lines 39+).

Regarding claim 15, Gowda '168 discloses a camera system (i.e., col. 1, lines 20-25) using a solid-state imaging element as an imaging device, said solid-state imaging element (i.e., Figs. 2 an 3A), comprising:

unit pixels, arranged in a matrix form (i.e., Figs. 2 and 3A; the elements 18 and 30), which have photoelectric transfer elements (6/26), transfer switches (8/22) for transferring charges stored in said photoelectric transfer elements (6/26), charge stored parts for storing charges (i.e., Figs. 1 and 3B; the elements' 7 and 25; col. 1, lines 65+ and col. 5, lines 50+) transferred by said transfer switches (8/22), reset switches (11/21) for resetting said charge store parts (7/25), and amplifying elements (13/23) for outputting signals in accordance with the potential of said charge store parts to vertical signal lines (15/15j);

a vertical scanning circuit (Figs. 2 and 3, the elements' 14 and 14') for selecting pixels in units of rows (18/30) by controlling a reset potential afforded to said reset switch (11/21);

a horizontal scanning circuit (Figs. 2 and 3A; the elements' 28 and 31_1 to 31_N; col. 1, lines 50+ col. 4, lines 15+, and col. 5, lines 30+) for sequentially selecting signals output to said vertical signal lines in units of columns (i.e., see col. 4, lines 35+); and

an output circuit for outputting signals (i.e., Figs. 2 and 3A; the elements' 31_1 to 31_N and 16; col. 1, lines 50+ and col. 6, lines 8+) selected by said horizontal scanning circuit via

horizontal signal lines (i.e., noted the bus lines connected between the elements 28 and 31 as shown in Figs. 2 and 3A).

7. Claims 1-3, 5, 12-13 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Hamasaki (U.S. 5,793,423).

Regarding claim 1, Hamasaki '423 discloses a solid-state imaging element (Fig. 2, col. 1, lines 10+), comprising: unit pixels, arranged in a matrix form (Fig. 2; the elements 5), which have photoelectric transfer elements (i.e., noted the photo sensors as shown in Fig. 2), transfer switches (Fig. 2, the elements 1 & 2) for transferring charges stored in said photoelectric transfer elements, charge store parts for storing charges transferred by said transfer switches (i.e., col. 3, lines 20-30), reset switches (3) for resetting said charge store parts (FD), and amplifying elements (4) for outputting signals in accordance with the potential of said charge store part to vertical signal lines (9) (see Fig. 2, col. 3, lines 20+);

a vertical scanning circuit (8) for selecting the pixels in units of rows by controlling a reset potential afforded to said reset switches (i.e., col. 3,lines 35+);

a horizontal scanning circuit (19) for sequentially selecting signals output to said vertical signal lines in units of columns (i.e., col. 4, lines 8+); and

an output circuit (col. 4, lines 19+) for outputting signals selected by said horizontal scanning circuit (19) via horizontal signal lines (Fig. 2, the elements' 15 and 19).

Regarding claim 2, Hamasaki '423 discloses wherein said vertical scanning circuit (8) affords vertical selection pulses sequentially output during vertical scanning to said reset switches as a reset potential thereof (col. 3, lines 35+).

Regarding claim 3, Hamasaki '423 discloses wherein said charge stored part is floating diffusion (col. 3, lines 28+).

Regarding claim 5, Hamasaki '423 discloses wherein said output circuit outputs signals read into said vertical signal lines in voltage mode (i.e., col. 4, lines 31+).

Regarding claim 12, Hamasaki '423 discloses a method for driving a solid-state imaging element (Fig. 2) including unit pixels, arranged in a matrix form (Fig. 2, the element's 5), which have photoelectric transfer elements (i.e., noted the photo sensor is part of the element 5 as shown in Fig. 2), transfer switches (i.e., the elements' 1 and 2) for transferring charges stored in said photoelectric transfer elements, charge stored parts for storing charges (i.e., col. 3, lines 20-30) transferred by said transfer switches (i.e., the elements' 1 and 2), reset switches (3) for resetting said charge store parts (FD), and amplifying elements (4) for outputting signals in accordance with the potential of said charge store parts to vertical signals lines (9), said method comprising the step of:

selecting pixels in units of rows by controlling a reset potential afforded to said reset switches (i.e., col. 3, lines 25+).

Regarding claim 13, Hamasaki '423 discloses the step of: outputting signals read into said vertical signal lines in voltage mode (col. 4, lines 31+).

Regarding claim 15, Hamasaki '423 discloses a camera system using a solid-state imaging element as an imaging device (Fig. 2; col. 1, lines 10+), said solid-state imaging element, comprising:

unit pixels, arranged in a matrix form (Fig. 2, the elements' 5), which have photoelectric transfer elements (i.e., noted the photosensors are part of the element 5 as shown in Fig. 2), transfer switches (i.e., the elements' 1 and 2) for transferring charges stored in said photoelectric transfer elements, charge stored parts for storing charges (i.e., col. 3, lines 20-30) transferred by said transfer switches (i.e., the elements' 1 and 2), reset switches (3) for resetting said charge store parts (FD), and amplifying elements (4) for outputting signals in accordance with the potential of said charge store parts to vertical signal lines (9);

a vertical scanning circuit (8) for selecting pixels in units (5) of rows by controlling a reset potential afforded to said reset switch (i.e., col. 3, lines 30+);

a horizontal scanning circuit (19) for sequentially selecting signals output to said vertical signal lines (9) in units of columns (col. 4, lines 5+); and

an output circuit for outputting signals (i.e., col. 4, lines 20+) selected by said horizontal scanning circuit (19) via horizontal signal lines (i.e., the elements' 15 and 19 as shown in Fig. 2).

8. Claims 1-3, 6, 8, 12, and 14-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Pain et al. (U.S. 5,886,659).

Regarding claim 1, Pain '659 discloses a solid-state imaging element (Figs. 1A-1C, 3A and 4; col. 3, lines 55+ and col. 6, lines 10+), comprising: unit pixels, arranged in a matrix form (i.e., Fig. 4, the pixel 410), which have photoelectric transfer elements (i.e., Figs. 2A and 3A; the elements' 210 and 310), transfer switches for transferring charges (i.e., Fig. 3a, the element 320) stored in said photoelectric transfer elements (310), charge store parts (FD) for storing charges transferred by said transfer switches (i.e., see Fig. 3A; col. 6, lines 25+), reset switches (i.e., Fig. 3A; the element 340) for resetting said charge store parts (FD), and amplifying elements (i.e., Fig. 3A; the element 360; col. 3, lines 55-60) for outputting signals in accordance with the potential of said charge store part to vertical signal lines (i.e., Figs. 3A and 4; col. 6, lines 25+);

a vertical scanning circuit (Fig. 4, the element 412) for selecting the pixels in units (410) of rows by controlling a reset potential afforded to said reset switches (i.e., col. 6, lines 24+);

a horizontal scanning circuit (Fig. 4; the elements' 414 and 420) for sequentially selecting signals output to said vertical signal lines in units of columns (i.e., col. 6, lines 25+); and

an output circuit (Fig. 4, the elements' 420 and 430) for outputting signals selected by said horizontal scanning circuit via horizontal signal lines (i.e., col. 6, lines 25+).

Regarding claim 2, Pain '659 discloses wherein said vertical scanning circuit (Figs. 3A and 4; the element's 412) affords vertical selection pulses sequentially output during vertical scanning to said reset switches as a reset potential thereof (i.e., col. 6, lines 2+).

Regarding claim 3, Pain '659 discloses wherein said charge stored part is floating diffusion (col. 6, lines 30+).

Regarding claim 6, Pain '659 discloses wherein said output circuit outputs signals read into said vertical signal lines in current mode (i.e., col. 6, lines 25+).

Regarding claim 8, Pain '659 discloses wherein a negative potential is applied to the control electrode of said transfer switches (i.e., col. 6, lines 40-43).

Regarding claim 12, Pain '659 discloses a method for driving a solid-state imaging element (Figs. 1A-1C, 3A and 4) including unit pixels, arranged in a matrix form (i.e., Fig. 4, the pixel 410), which have photoelectric transfer elements (i.e., Figs. 2A and 3A; the elements' 210 and 310), transfer switches (i.e., Fig. 3A, the element 320) for transferring charges stored in said photoelectric transfer elements (310), charge stored parts (FD) for storing charges transferred by said transfer switches (i.e., see Fig. 3A; col. 6, lines 25+), reset switches for resetting (i.e., Fig. 3A; the element 340) said charge store parts (FD), and amplifying elements for outputting signals (i.e., Fig. 3A; the element 360; col. 3, lines 55-60) in accordance with the potential of said charge store parts to vertical signals lines (i.e., Figs. 3A and 4; col. 6, lines 25+), said method comprising the step of:

selecting pixels in units of rows (Fig. 4, the element's 410) by controlling a reset potential afforded to said reset switches (Figs. 3A and 4; col. 6, lines 2+).

Regarding claim 14, Pain '659 discloses the step of: outputting signals read into said vertical signal lines in current mode (i.e., col. 6, lines 25+).

Regarding claim 15, Pain '659 discloses a camera system using a solid-state imaging element as an imaging device (Figs. 2A, 3A and 4; col. 3, lines 55+ and col. 6, lines 10+), said solid-state imaging element, comprising:

unit pixels, arranged in a matrix form (i.e., Fig. 4, the pixel 410), which have photoelectric transfer elements (210/310), transfer switches for transferring charges (i.e., Fig. 3A, the element 320) stored in said photoelectric transfer elements (310), charge stored parts (FD) for storing charges transferred by said transfer switches (i.e., see Fig. 3A; col. 6, lines 25+), reset switches for resetting (i.e., Fig. 3A; the element 340) said charge store parts (FD), and amplifying elements for outputting signals (i.e., Fig. 3A; the element 360; col. 3, lines 55-60) in accordance with the potential of said charge store parts to vertical signal lines (i.e., Figs. 3A and 4; col. 6, lines 25+);

a vertical scanning circuit (Fig. 4, the element 412) for selecting pixels in units of rows (410) by controlling a reset potential afforded to said reset switch (i.e., col. 6, lines 26+);

a horizontal scanning circuit (Fig. 4, the elements 414/420) for sequentially selecting signals output to said vertical signal lines in units of columns (i.e., col. 6, lines 25+); and

an output circuit for outputting signals (Fig. 4, the elements' 420 and 430) selected by said horizontal scanning circuit via horizontal signal lines (i.e., col. 6, lines 25+).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
> This application currently names joint inventors.

In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda '168 in view of Miwada (U.S. 5,206,932).

Regarding claim 4, it is noted that Gowda '168 does not explicitly state that the reset switches comprise a depression type transistor.

However, the above mentioned claimed limitations are well-known in the art as evidenced by Miwada '932. In particular, Miwada '932 teaches the use of a depression type transistor in the solid-state imaging device as a reset switch (Fig. 1; col. 4, lines 50-55) for

resetting the floating diffused region (7) so that deterioration of the dynamic range is prevented (i.e., see col. 3, lines 1-5).

In view of the above, having the system of Gowda '168 and then given the well-established teaching of Miwada '932, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Gowda '168 as taught by Miwada '932, since Miwada '932 states at column 3, lines 3+ that such a modification would prevent the solid-state imaging device from deterioration of the dynamic range resulting from faulty resetting of the floating diffused region thereof.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Ishida '971, Zhou '871, Sauer '758, Shinohara '884, Ackland '141 and Fossum '483 shows a solid-state imaging element having unit pixels, a vertical scanning circuit, a horizontal scanning circuit and the output circuit thereof.

b. Tower '371 shows a solid-state imaging element, wherein a negative potential is applied to the control electrode of the transfer switches (i.e., see col. 5, lines 15+).

c. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Aung S. Moe** whose telephone number is **(703) 306-3021.** If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Wendy Garber**, can be reach on (703) 305-4929.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to the customer service number **(703) 306-0377.**

AUNG S. MOE
PATENT EXAMINER

A. Moe

July 10, 2003